CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor device on a semiconductor substrate, comprising:

forming a gate dielectric on the semiconductor substrate;

forming a gate stack overlying the gate dielectric, the gate stack having a sidewall, wherein the gate stack comprises a conductive layer and a hard mask overlying the conductive layer;

selectively depositing a liner over the gate stack such that the liner is deposited on the hard mask at a rate lower than the rate of deposition on the conductive layer, so that the liner is thinner on the hard mask than on the conductive layer; and

forming a nitride spacer over the liner.

2. The method of claim 1, wherein said forming a nitride spacer comprises:

forming a layer of nitride spacer material conformally over the liner; and

etching back the layer of nitride spacer material.

3. The method of claim 1, wherein the liner is deposited on the hard mask at a rate approximately one-fifth the rate of deposition on the conductive layer.

4. The method of claim 1, wherein the liner is deposited selectively on the conductive layer in a thickness at least twice a thickness of deposition on the hard mask.

5. The method of claim 1, wherein said liner is formed of oxide.

6. A gate structure, comprising:

a gate dielectric on a semiconductor substrate;

a gate stack overlying the gate dielectric, the gate stack having a sidewall, wherein the gate stack comprises a conductive layer and a hard mask overlying the conductive layer;

an oxide liner disposed on the sidewall of the gate stack, wherein the

thickness of the liner is substantially thicker on the conductive layer than on the hard mask, the liner having a step along the boundary of the hard mask and the conductive layer;

a nitride sidewall spacer disposed over the liner and sloped away from the gate stack adjacent the gate dielectric.

7. The gate structure of claim 6, further comprising:

a PMD layer overlying the gate stack, the nitride spacer, and the capping layer.

8. The gate structure of claim 7, further comprising:

a contact plug formed within the PMD layer adjacent the gate stack.

9. The device of claim 6 wherein said hard mask includes one or more layers of material selected from the group consisting of oxide, nitride and oxynitride.

10. A semiconductor device, comprising:

at least two adjacent gate stacks over a semiconductor substrate, the adjacent gate stacks each having a sidewall opposing each other, wherein each of the gate stacks comprises a conductive layer and a hard mask overlying the conductive layer;

a liner selectively deposited overlying opposing sidewalls of the gate stacks , the liner being thinner on the hard mask than on the conductive layer, the liner having a step along the boundary of the hard mask and the conductive layer; and

at least two adjacent nitride sidewall spacers on the liner each overlying the opposing sidewalls.

11. The device of claim 10, wherein the at least two adjacent sidewall spacers have a bottom, middle, and top space therebetween, and wherein the bottom space is substantially shorter than the middle space.

12. The device of claim 10, wherein the top space is wider than the middle space.

13. The device of claim 10, wherein the gate stacks and closely spaced to

provide a gap between them, and the gate stacks, liner and sidewall spacers are covered by a PMD layer, a portion of the PMD layer filling the gap.

14. The device of claim 10, wherein the portion of the PMD layer filling the gap being free of voids.

15. The device of claim 10 wherein said hard mask includes one or more layers of material selected from the group consisting of oxide, nitride and oxynitride.

16. A method of manufacturing a semiconductor device on a semiconductor substrate, comprising:

forming at least two adjacent gate stacks over the substrate, the adjacent gate stacks each having a sidewall opposing each other,

wherein each of the gate stacks comprises a conductive layer and a hard mask overlying the conductive layer;

selectively depositing a liner over the gate stacks, so that the liner is thicker on the conductive layer than on the hard mask; and

forming adjacent at least two nitride spacers on the liner, overlying the opposing sidewalls,

wherein the liner is deposited over the hard mask at a rate lower than the rate of deposition on the conductive layer.

17. The method of Claim 16, wherein the liner is deposited on the hard mask at a rate approximately one-fifth the rate of deposition on the conductive layer.

18. The method of Claim 16, wherein the liner is deposited selectively on the conductive layer in a thickness at least twice a thickness of deposition on the hard mask.

19. The method of Claim 16, wherein said forming adjacent nitride spacers comprises:

forming a layer of nitride spacer material conformally over the liner, and etching back the layer of nitride spacer material.

20. The method of claim 16, wherein the adjacent nitride spacers have top, middle, and bottom spaces therebetween, and wherein the bottom space is substantially shorter than the middle space.